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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,650	11/09/2001	Derek Ward	P67300US0	5599
136	7590	04/15/2008	EXAMINER	
JACOBSON HOLMAN PLLC 400 SEVENTH STREET N.W. SUITE 600 WASHINGTON, DC 20004				JARRETT, RYAN A
ART UNIT		PAPER NUMBER		
2121				
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			04/15/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/986,650	WARD, DEREK	
	<b>Examiner</b>	<b>Art Unit</b>	
	Ryan A. Jarrett	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 March 2008.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 3,4,8-19 and 22-32 is/are pending in the application.
- 4a) Of the above claim(s) 8-19,23-26 and 29-32 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 3,4,22,27 and 28 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

### *Election/Restrictions*

Claims 8-19, 23-26, 29, and 30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/05/07.

Newly submitted claims 31 and 32 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The originally claimed invention, in its most limiting sense (claims 27 and 28), is directed to program swapping with programmable logic hardware being arranged in sections separately configurable, including circuits to support relocation of user program circuit state data. Newly submitted claim 31 is directed to program swapping within a single section of programmable hardware, which is clearly distinct from program swapping between two sections of programmable hardware. These two inventions could also be considered subcombinations. And newly submitted claim 32 is directed to failure protection, also clearly distinct from the originally claimed invention.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 31 and 32 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

***Priority***

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in New Zealand on 11/9/00. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

***Specification***

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The following limitations appear to have no literal support in the original disclosure as filed:

the “subsystems”, “first subsystem”, and “second subsystem” of claims 3 and 4;  
the “dual purpose” flip-flops of claim 3;  
the “shift chain” of claim 3;  
the “clock to said dual purpose flip-flops is enabled” of claim 4;  
the “pause mode in which the clock to said dual purpose flip-flops is disabled” of claim 4; and  
the particular functionality recited in claims 22, 27, and 28.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 3, 4, 22, 27, and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The following limitations appear to have no literal support in the original disclosure as filed:

the “subsystems”, “first subsystem”, and “second subsystem” of claims 3 and 4;  
the “dual purpose” flip-flops of claim 3;  
the “shift chain” of claim 3;  
the “clock to said dual purpose flip-flops is enabled” of claim 4;  
the “pause mode in which the clock to said dual purpose flip-flops is disabled” of claim 4; and  
the particular functionality recited in claims 22, 27, and 28.

Claims 3, 4, 22, 27, and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3 line 20, the phrase "configured including" is fragmented and/or unclear.

Claim 4 recites the limitation "the monitoring computer" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claims 22, 27, and 28 depend from claims 3 and 4 and incorporate the same deficiencies.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3, 4, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by “Virtex-E 1.8 V FPGAs: Preliminary Product Specification”. Xilinx (9/20/00) DS022 v1.7. (hereinafter referred to as “Virtex-E”)

For example, per claim 3, Virtex-E discloses an FPGA in which programmable logic hardware is configured including at least two functionally separate subsystems, a first subsystem comprising said user program circuit, and a second subsystem to provide monitoring services and to control the operation of said user program circuit, wherein:

    said first subsystem has a plurality of flip-flops combined with gating circuits, wherein one of said flip-flops combined with one of said gating circuits forms a dual purpose flip-flop for storing state data in said user program circuit, said dual purpose flip-flops, when connected in said user program circuit, are selectively operable in a first way as a shift chain operable to provide both read and write access to said state data or in a second way as logic elements of said user program circuit, only one of said first way or said second way being operative at any one time (e.g., pg. 19: “Readback”, pg. 14: “For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple

modifications can be downloaded into the system in a matter of minutes.”, pg. 10: “The TAP also supports two internal scan chains and configuration/readback of the device”, pg. 12: “Data Registers” section).

Per claim 4, Virtex-E discloses the programmable controller as claimed in claim 3, wherein,

said second subsystem enables the control and operation of said user program circuit in a plurality of modes of operation in response to commands from the monitoring computer, said modes of operation including:

a logic processing mode in which said dual purpose flip-flops are operated as said logic elements in said user program circuit, and in which the clock to said dual purpose flip-flops is enabled (e.g., pg. 14: “single-step the logic”), or

a pause mode in which the clock to said dual purpose flip-flops is disabled (e.g., pg. 14: “single-step the logic”),

and wherein either said logic processing mode or said pause mode may be temporarily interrupted by a data access mode in which said dual purpose flip-flops are operated as part of a shift chain so that enabling the clock to said dual purpose flip-flops shifts the state data in said dual purpose flip-flops and provides both read and write access (e.g., pg. 14: “readback the contents of the flip-flops”).

Per claim 22, Virtex-E discloses the ability to enter a data access mode from either a logic processing mode or a pause mode (e.g., pg. 19: “real-time debugging”, “The sequence can also be paused at any stage”).

It further noted that there is a serious question as to the limiting nature of some of the functional language that Applicant has extensively employed in claims 3, 4, and 22, since apparatus claims must be structurally distinguishable from the prior art. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). “[A]pparatus claims cover what a device is, not what a device does.” *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original). See MPEP 2114.

Further, the manner of operating the device does not differentiate an apparatus claim from the prior art. A claim containing a “recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Additionally, language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim: (A) statements of intended use or field of use (i.e.,

"may", "can", "able", "enable"), (B) "adapted to" or "adapted for" clauses, (C) "wherein" clauses, or (D) "whereby" clauses. See MPEP 2111.04.

It would appear that Applicant's claims would be better written as method claims in order to capture all of the desired functionality currently being claimed.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virtex-E as applied to claim 22 above, and further in view of New et al. US 6,091,263.

Virtex-E does not appear to explicitly disclose means to support relocation of state data during a program swap operation.

New et al. discloses a rapidly reconfigurable FPGA comprising means to support relocation of state data during a program swap operation, as recited in claims 27 and 28 (e.g., col. 8 line 13 – col. 10 line 30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Virtex-E with New et al. since New et al. teaches that enabling state data values to be saved and restored from different local cache memories advantageously expands the configuration and reconfiguration possibilities of the configurable logic block (col. 9 lines 7-10).

It further noted that there is a serious question as to the limiting nature of some of the functional language that Applicant has extensively employed in claims 27 and 28, since apparatus claims must be structurally distinguishable from the prior art. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128

F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). “[A]pparatus claims cover what a device is, not what a device does.” Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original). See MPEP 2114.

Further, the manner of operating the device does not differentiate an apparatus claim from the prior art. A claim containing a “recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Additionally, language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim: (A) statements of intended use or field of use (i.e., “may”, “can”, “able”, “enable”), (B) “adapted to” or “adapted for” clauses, (C) “wherein” clauses, or (D) “whereby” clauses. See MPEP 2111.04.

It would appear that Applicant's claims would be better written as method claims in order to capture all of the desired functionality currently being claimed.

***Response to Arguments***

Applicant's arguments, see page 17 line 12 – page 19 line 22, filed 03/06/08, with respect to the rejection of claims 3, 4, and 22 under 35 U.S.C. 102(b) as being anticipated by Virtex-E have been fully considered but they are not persuasive, since Virtex-E discloses an internal scan chain for accessing the flip-flop state data (e.g., pg. 19: “Readback”, pg. 14: “For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.”, pg. 10: “The TAP also supports two internal scan chains and configuration/readback of the device”, pg. 12: “Data Registers” section).

Applicant's arguments, see page 19 line 23 – pg. 20 line 5, filed 03/06/08, with respect to claims 3, 4, 22, 27, and 28 have been fully considered and are persuasive. The rejection of claims 3, 4, 22, 27, and 28 under 35 U.S.C. 102(b) as being anticipated by New et al. has been withdrawn.

Applicant's arguments, see page 20-21, filed 03/06/08, with respect to the rejection of claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over Virtex-E in view of New have been fully considered but they are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, New et al. teaches that enabling state data values to be saved and restored from different local cache memories advantageously expands the configuration and reconfiguration possibilities of the configurable logic block (col. 9 lines 7-10).

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (571) 272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan A. Jarrett/  
Primary Examiner, Art Unit 2121

04/12/08